REMARKS

The Examiner rejected claims 2-5 and 12-15 under 35 U.S.C. §102(b) as allegedly being anticipated by US Patent No. 5,646,563, issued to Kuo.

The Examiner rejected claims 6-10 and 16-20 under 35 U.S.C. §103(a) as allegedly being unpatentable over US Patent No. 5,646,563, issued to Kuo.

Applicants respectfully traverse the §102 and §103 rejections with the following arguments.

35 U.S.C. §102

Claims 2-5 and 12-15 are rejected under 35 U.S.C. §102(b) as allegedly being anticipated by US Patent No. 5,646,563, issued to Kuo.

The Examiner alleges that "As per claim 2, Kuo discloses a PLL (Fig. 4), comprising: a voltage controlled oscillator (VCO 440) for providing a first signal (VCO IN); a phase comparator (310) for comparing the first signal (VCO_IN) to a reference signal (REF IN) and providing a control signal (CNTRL N and CNTRL P); and a charge pump circuit (320) comprising a current source (340), a first FET (328), a first capacitor (C1) wherein the first FET, second PET and first capacitor electrically coupled (as shown, they are electrically connected in the charge pump circuit 340), wherein the current source is directly connected to the source of the first FET (as shown, the current source 340 is directly connected to VSS and the source of the first FET 328 is also directly connected to VSS), wherein the second FET comprises a parasitic capacitance (every FET has this element when the FET is operated in a switching environment), wherein the charge pump circuit is for receiving the control signal (CNTRL N and CNTRL P) and performing the recited function (any PLL performs the recited function), and wherein the second FET comprises parasitic capacitance that is to direct the spark current to ground (the frequency of noise, i.e.,jitters or spark current are noise, caused by the switching action is much higher than the switching frequency, and therefore, parasitic capacitance exists between terminals of the second FET to groundd this parasitic capacitance acts as a filter to direct the jitters to ground), the charge pump circuit compensates for a spark current resulting from a switching mode of the control signal (column 4, lines 1-14,

i.e., the structure of the charge pump 320 is for reducing the jitters (spark current) caused by the switching of the control signal) ".

As to claims 2 and 12, Applicant respectfully contends that Kuo does not anticipate claims 2 and 12, because Kuo does not teach each and every feature of claims 2 and 12. For example, Applicant respectfully contends that Kuo does not teach the feature of " and wherein the second FET is adapted to be operated such that a **spark current** resulting from a switching mode of the control signal is directed through the parasitic capacitance to ground " (emphasis added). Kuo does not teach **spark current** as taught by Applicant's claims 2 and 12. In contrast, Kuo teaches in col. 4, lines 10-12 " **jitter** in output voltage Vout ". Applicant contends that the Examiner has incorrectly concluded that the **jitter** in Kuo is the same as the **spark current** in Applicant's claims 2 and 12. Applicant teaches in claims 2 and 12 that spark current results from a switching mode of a control signal. A spark is defined in The Modern Dictionary of Electronics by Rudolf F. Graph as "a single, short electrical discharge ". Kuo attributes jitter in col. 1, line 25 to "output voltage fluctuations" Kuo teaches in col. 2, lines 15-17 " Voltage Vout increases and decreases **repeatedly** in this manner causing jitter in the signal provided by the VCO 140 ". Kuo further teaches in Col. 2, lines 20-23, that "Another source of jitter in voltage Vout and the signal provided by VCO 140 is relative fluctuations between supply voltage Vdd or reference voltage Vss ". Therefore, Applicant contends that the **spark current** (i.e., a single, short electrical discharge) in Applicant's claims 2 and 12 is distinguished from the **jitter** (i.e., output voltage fluctuations) in Kuo. Based on the preceding argument, Applicant respectfully maintains that Kuo does not anticipate claims 2 and 12, and that claims 2 and 12 are in condition for allowance. Since claims 3-10 depend from claim 2 and claims 13-20 depend

from claim 12, Applicants contend that claims 3-10 and 13-20 are likewise in condition for allowance.

35 U.S.C. §103

Claims 6-10 and 16-20 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over US Patent No. 5,646,563, issued to Kuo.

The Examiner alleges that "As per claim 6, Kuo discloses a PLL as discussed in claim 2 but he does not explicitly disclose the second FET is adjusted to operate in saturation mode as called for in the claim (actually, Kuo does not mention whether the first FET (326) is operated in saturation mode).

However, as ruled by the court, when a general condition is met, it is not inventive to modify the parameter to obtain the optimum result. In this instant case, Kuo teaches a PLL having the structure recited in claim 2 (general condition), the act of increasing and/or decreasing the current value of the current source (340) which resulting in driving the second FET (326) to saturation mode to obtain the optimum result is well within the level of one skilled in the art.

It would have been obvious to one skilled in the art at the time of the invention was made to adjust the current source (340) in the Kuo's PLL so that the second FET is operated in saturation mode for the motivation to obtain the optimum result is well within the level of one

saturation mode for the motivation to obtain the optimum result is well within the level of one skilled in the art, i.e., by experiment, one skilled in the art can easily vary the value of the current

source to find a value which will minimize the spark current using the structure taught by Kuo.As per claim 7, the recited direct current voltage is the voltage at the gate of the second

FET (326), and since the second FET is in saturation mode, the recited condition on the last three lines must be met.

As per claims 8-10, these claims are rejected for the same reasons and motivations as discussed in claim 6 herein above, i.e., Kuo explicitly discloses the structure as discussed in claim 2, it is not inventive to modify the paramcters as recited in these claims to obtain the optimum conditions.

As per claims 16-20, those claims are rejected for the same reasons and motivation noted in claims 6-10, respectively".

As to claims 6 ands 16, Applicant respectfully contends that claims 6 and 16 are not unpatentable over Kuo because Applicant contends that the Examiner has not provided a persuasive argument as to why claims 6 and 16 are unpatentable over Kuo. The Examiner alleges that "As per claim 6, Kuo discloses a PLL as discussed in claim 2 but he does not explicitly disclose the second FET is adjusted to operate in saturation mode as called for in the claim (actually, Kuo does not mention whether the first FET (326) is operated in saturation mode) ... However, as ruled by the court, when a general condition is met, it is not inventive to modify the parameter to obtain the optimum result. In this instant case, Kuo teaches a PLL having the structure recited in claim 2 (general condition), the act of increasing and/or decreasing the current value of the current source (340) which resulting in driving the second FET (326) to saturation mode to obtain the optimum result is well within the level of one skilled in the art".

In response, Applicant cites *In re Antonie*, 559 F.2d 618, 619, 195 U.S.P.Q. 6, 8 (C.C.P.A. 1977) which held that varying a variable to optimize a result is obvious only if the prior art has disclosed that the variable is a result effective variable for optimizing the result. In application to claims 6 and 16, the Examiner has not provided any evidence from the prior art demonstrating that "increasing and/or decreasing the current value of the current source ... result[s] in driving the second FET ... to saturation mode." In other words, the Examiner has not cited any prior art demonstrating that it was known to a person of ordinary skill in the art that the value of the current source is a result effective variable with respect to the alleged optimization.

As to claims 8 and 18, Applicant respectfully contends that claims 8 and 18 are not unpatentable over Kuo because Kuo does not teach or suggest the following feature of claims 8 and 18 "a saturation current value of the second FET is **greater** that a saturation current value of the current source" (emphasis added). The Examiner suggests (in rejection of claim 6, claim 8 is dependnet upon claim 6) " It would have been obvious to one skilled in the art at the time of the invention was made to adjust the current source (340) in the Kuo's PLL so that the second FET is operated in saturation mode ". If as the Examiner suggests, the current source 340 in Kuo could be adjusted to operate the second FET 326 in saturation mode then Applicant contends that the saturation current value of the second FET would have to be **less** than the saturation current value of the current source 340 so that the current source would comprise enough current to drive the second FET 326 in saturation mode. Applicant's claims 8 and 18 actually teach saturation current value of the second FET **greater** that a saturation current value of the current source. Therefore, Applicant contends that the Examiner's argument is not persuasive. Accordingly, Applicant contends that claims 8 and 18 are not unpatentable over Kuo.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or Deposit Account 09-0456.

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